IN THE DRAWINGS

Figure 7 has been amended to change step 720 from "Any Conflicting Instruction Requests?" to "Any Conflicting Instruction Requests Detected By Being Associated With Same Group Of Cache Sets?"

Also, step 750 has changed from "Forward Selected Instruction Request Using Round-Robin Arbitration" to "Forward Selected Instruction Request Using Round-Robin Arbitration And Increment Priority Indication Of Unselected Priority Request."

Finally, indications of "Yes" and "No" were added to the decision branches of step 730.

REMARKS

Claims 1-48 were presented for examination and were pending in this application. In an Official Action mailed April 10, 2006, claims 1-7, 10-12, 14-27, 30-38 and 43-46 were rejected and claims 8-9, 28-29 and 39-40 were objected to (Office Action Summary also indicates that claims 13, 41-42 and 47-48 were allowable, although text within the Official Action indicates that these claims were rejected). As listed above, Applicant herein amends claims and Applicant herein cancels claims, without prejudice. Applicant now requests reconsideration and allowance of all listed claims.

Applicant thanks Examiner for examination of the claims pending in this application and addresses Examiner's comments below.

In paragraph 4 of the Official Action, Examiner objected to drawings under 37 CFR 1.83(a) because two claimed limitations were allegedly now shown in the drawings. In response, Applicant has amended Figure 7 as described above to more clearly illustrate the claimed limitations. The amendments to the drawings add no new matter. Accordingly, Applicant respectfully obviates the objection.

In paragraph 9 of the Official Action, Examiner rejected independent claims 1 and 16 under 35 USC 103(a) as being unpatentable over Joy (US 6,507,862) in view of Ebner (US 6,928,525). However, in paragraph 60, Examiner indicated that claims 8-9 would be allowable if rewritten in independent form. To traverse the rejection, Applicant has amended independent claims 1 and 16 to recite some limitations of allowable claims 8-9 (i.e., an instruction request arbiter and a means for arbitration that control instruction requests by "broadcasting the traffic mode to the plurality of processor clusters").

More specifically, Joy discloses a processor including logic for attaining a very fast exception handling functionality. (Abstract). An external cache control unit 922 (see also ECU 1022 and ECU Arbiter 1125) disclosed by Joy manages instruction cache and data cache misses by allowing access to the external cache in alternating clock cycles. (See 19:65-20:2). Meanwhile, Ebner discloses a semaphore mechanism in a multiport cache memory system that allows concurrent access to a cache memory. (Abstract). When at least two requests for the same line are received, Ebner discloses that a cache arbiter selects between requesters and grants access to the requests line. (Fig. 4).

However, both Joy and Ebner, either alone or in combination, fail to teach or suggest broadcasting the traffic mode to a plurality of processor clusters to control access of processing clusters, as recited in amended claims 1 and 16. Joy uses a passive ECU that merely alternates clock cycles to allow access to the external cache. Likewise, Ebner uses a passive cache arbiter to select between requesters. Neither of the disclosed devices broadcast a traffic mode to control access in an active manner. Thus, independent claims 1 and 16, as amended, and all related dependent claims are patentable over Joy and Ebner either alone or in combination.

In paragraph 29 of the Official Action, Examiner rejected independent claims 21, 32 and 43 over Joy in view of Ebner, and further in view of Yu (US 6,345,345). Again, Examiner indicated that dependent claims 28-29 and 47-48 would be allowable if rewritten in independent form. These independent claims were amended to include some limitations of allowable claims 28-29 and 39-40, similar to the amendments of independent claims 1 and 16, as discussed above. Yu, in disclosing how to limit a number of allowed transmit data transfers within a PCI bus mastership period, fails to cure the deficiencies of Joy and Ebner.

Thus, independent claims 21, 32 and 43 are patentable over Joy, Ebner and Yu, either alone or in combination.

CONCLUSION

In sum, Applicant respectfully submits that the claims as presented herein, are patentably distinguishable over the cited reference (including references cited, but not applied). Therefore, Applicant requests reconsideration and allowance of these claims.

In addition, Applicant respectfully invites Examiner to contact Applicant's representative at the number provided below if Examiner believes it will help expedite furtherance of this application.

RESPECTFULLY SUBMITTED,
Donald E. Steiss, et al.

Date: July 10, 2006

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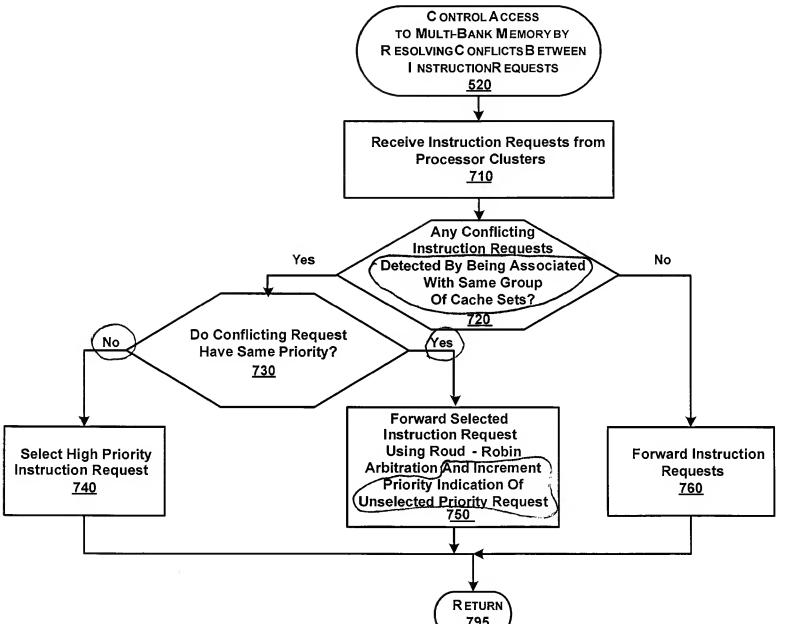
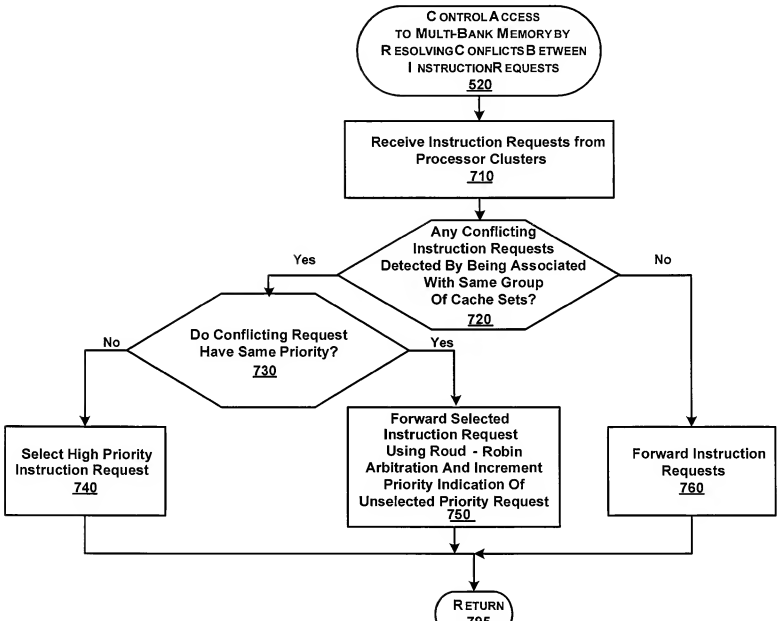

CONTROL ACCESS TO MULTI-BANK MEMORY BY RESOLVING CONFLICTS BETWEEN INSTRUCTION REQUESTS
520
Receive Instruction Requests from Processor Clusters
710
Any Conflicting Instruction Requests Detected By Being Associated With Same Group Of Cache Sets?
720
Yes
No
Do Conflicting Request Have Same Priority?
730
No
Yes
Select High Priority Instruction Request
740
Forward Selected Instruction Request Using Roud - Robin Arbitration And Increment Priority Indication Of Unselected Priority Request
750
Forward Instruction Requests
760
RETURN
795

FIG. 7


CONTROL ACCESS TO MULTI-BANK MEMORY BY RESOLVING CONFLICTS BETWEEN INSTRUCTION REQUESTS
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Receive Instruction Requests from Processor Clusters
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720
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No
Do Conflicting Request Have Same Priority?
730
No
Yes
Select High Priority Instruction Request
740
Forward Selected Instruction Request Using Roud - Robin Arbitration And Increment Priority Indication Of Unselected Priority Request
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760
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795

FIG. 7